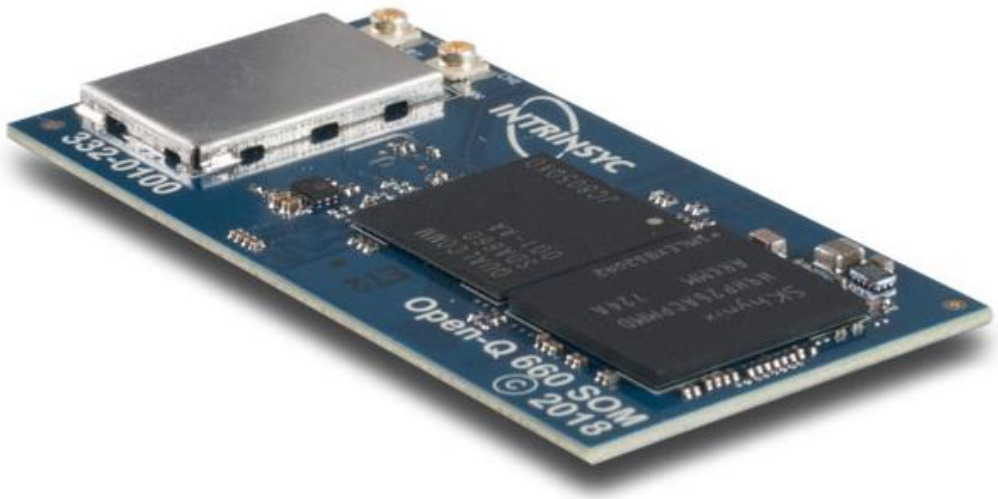

Open-Q 660 µSOM HW Device Specification

[Document: ITC-01RND1336-SOM-DS Version: 1.1]

Identification

Document Title	Open-Q 660 µSOM HW Device Specification
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History

REVISION	DATE	DESCRIPTION	PAGES
1.0	April 30, 2019	Initial Release	All
1.1	Oct 11, 2019	Add shipping information to section 7.3 Corrected typo in Table 12 Updated the SOM Operating Temperature rating	30 23 24

Table of Contents

1. INTRODUCTION

This document applies to the Open-Q 660 µSOM. Technical specifications for other SOMs in the Intrinsyc product line are covered under separate documents.

1.1 Purpose

The purpose of this document is to provide the technical specifications of the Intrinsyc Open-Q 660 µSOM.

1.2 Scope

This document covers the following information on the Open-Q 660 µSOM:

- Electrical and mechanical specifications
- SOM pin-out
- Device handling and packaging
- Ordering information.

1.3 Intended Audience

This document is intended for users who wish to understand the technical specifications of the Intrinsyc Open-Q 660 µSOM.

1.4 Acronyms and Abbreviations

Acronym / Abbreviation	Definition
ANT	ANTenna
BAT, BATT	BATTery
BAM	Bus Access Manager
BLSP	BAM-based Low-Speed Peripheral
BOM	Bill Of Materials
BT	Blue Tooth
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMI	Electro-Magnetic Interference
EN	ENable
ERM	Eccentric Rotating Mass
ESD	Electro-Static Discharge
GND	GrouND
GPIO	General Purpose I/O
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	INTerrupt
JTAG	Joint Test Action Group

Acronym / Abbreviation	Definition
LDO	Low Drop-Out
LRM	Linear Resonant Actuator
LTE	Long-Term Evolution
LPI	Low Power Island
MDP	Mobile Display Port
MI2S	Mobile Inter-IC Sound
MIC	MICrophone
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PWM	Pulse-Width Modulation
RF	Radio Frequency
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SDC	Secure Digital Interface
SOM	System On Module
SPI	Serial Peripheral Interface
SSC	Snapdragon Sensor Core
TX	Transmit
UART	Universal Asynchronous Receiver/Transmiter
UIM	User Interface Module
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

1.5 Signal Name Suffix

Suffix	Definition
_N	Indicates that the signal is ACTIVE LOW
_P/N	Identifies the two signals comprising a differential pair

2. DOCUMENTS

This section lists any parent and supplementary documents for the Open-Q 660 µSOM Device Specification. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-Q 660 µSOM

2.2 Reference Documents

Available at http://tech.intrinsyc.com (dev kit registration required)

REFERENCE	TITLE
R-1	Open-Q 660 µSOM Development Kit – User Guide
R-2	Open-Q 660 µSOM – Carrier Board Design Guide
R-3	Open-Q 660 µSOM Schematics (SOM and Carrier)
R-4	
R-5	

3. SUMMARY OF FEATURES

The Open-Q 660 µSOM contains the core of the Snapdragon 660 architecture. Measuring in at 50mm x 25mm, the SOM is where all the processing occurs. It connects to a carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting peripherals and interfaces on the platform.

3.1 SOM Block Diagram

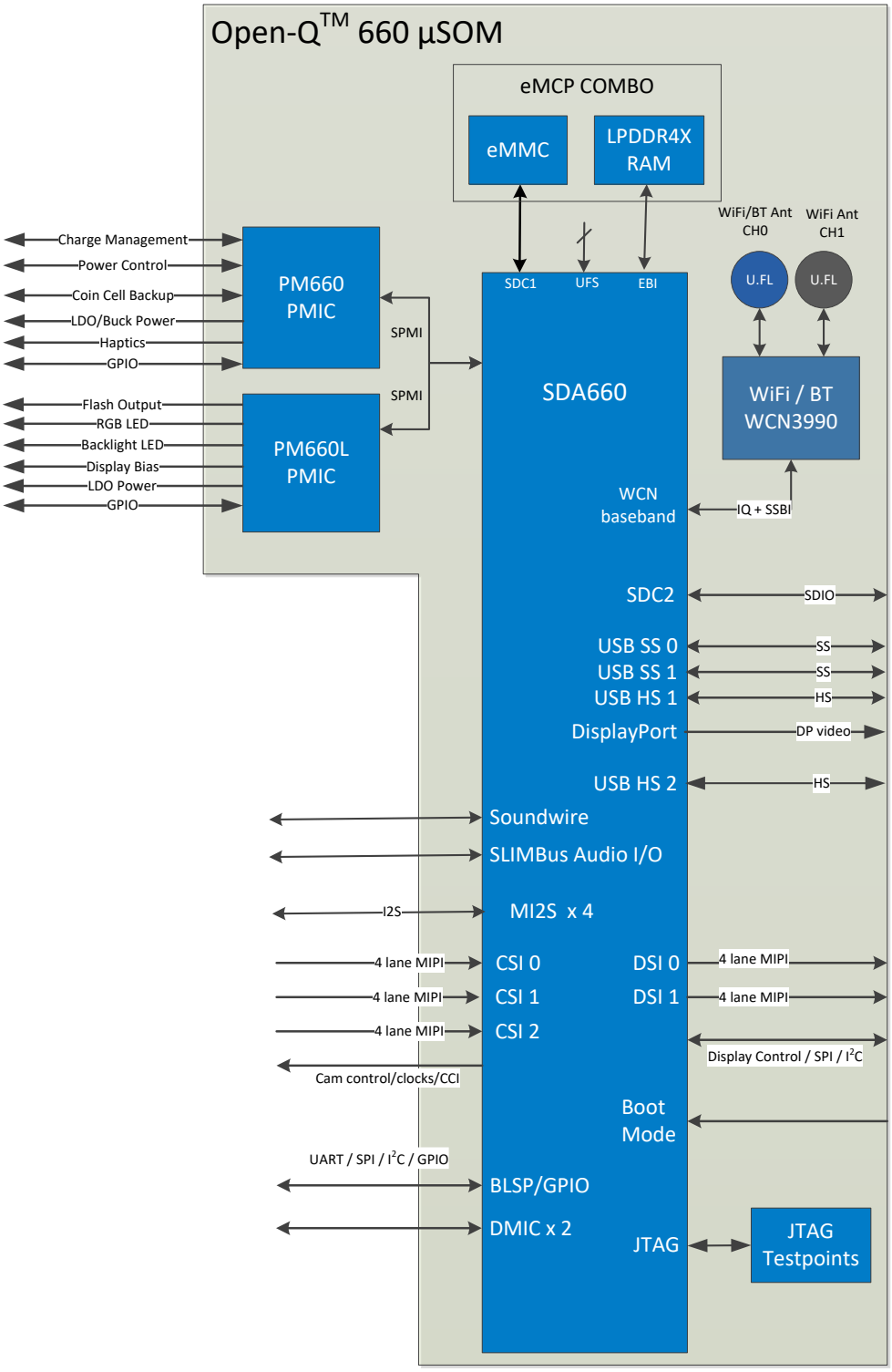

Figure 1 – Open-Q 660 µSOM Block Diagram

3.2 SOM Technical Specifications

See the table below for the Open-Q 660 µSOM technical specifications.

Table 1 – Open-Q 660 µSOM Technical Specifications

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	SDA660 CPU	Qualcomm Snapdragon 660 Processor	Qualcomm® Kryo™ 260 CPU, quad core, 64-bit up to 2.2GHz
	PM660 PMIC	Qualcomm Companion PMIC for 660 Processor	Power management, charging, general housekeeping, user interface, and IC level interface support
	PM660L PMIC	Qualcomm Companion PMIC for 660 Processor	Power management, general housekeeping, user interface, and audio codec
Memory	4GB LPDDR4X + 32GB eMMC	eMCP combo memory chip	LPDDR4X RAM eMMC V5.1 Flash storage
Connectivity	Wi-Fi 5Ghz/2.4GHz	Qualcomm WCN3990 WLAN / Bluetooth Wireless Connectivity IC	2x2 MIMO WLAN compliant with IEEE802.11 a/b/g/n/ac
	Bluetooth 2.4 GHz	Qualcomm WCN3990 WLAN / Bluetooth Wireless Connectivity IC	Compliant with Bluetooth version 5.x
RF Interfaces (see section below)	WLAN / BT	2 antenna connectors on SOM for 2x2 MIMO Wi-Fi. Bluetooth uses one of the 2 antenna ports.	2 x U.FL, 50 ohm coaxial connectors
Audio Interfaces	Digital MI2S	4 Digital MI2S ports	Three 2-bit ports, 1 4-bit port
	2x digital MIC Channels	Digital MIC (clock / data) inputs	Supports 2 digital mics per input = 4 total
	SLIMBUS	2 bit SLIMBUS port	Support for external audio codec
	SoundWire	Support for external smart speaker amplifier	
Digital Interfaces	MIPI CSI	Three 4-lane MIPI CSI Camera interfaces	(4/4/4 or 4/4/2/1) D-PHY 1.2 at 2.1 Gbps per lane or three 3-lane C-PHY 1.0 at 17 Gbps (2.5 G symbols per trio per second)
	MIPI DSI	Two 4-lane MIPI DSI Display interfaces	D-PHY 1.2 at 2.1 Gbps per lane and 1080p30 Miracast/4K30DP

Subsystem / Connectors	Feature Set	Description	Specification
	USB 2.0 host	1x USB 2.0 high-speed port	USB 2.0 high speed host
	USB 3.1 Type-C	Full USB 3.1 Type-C support with VESA DisplayPort output	USB 3.1
	SDIO	One 4-bit Secure Digital interface	Supports dual voltage SD card peripheral
	GPIO / I2C / SPI / UART	>100 configurable IO	See R-1 for list configurable IO through GPIO and BLSP exposed on the carrier board connectors
Connectors	3x 100-pin board to board connectors	3x Hirose 100-pin DF40C header connectors	300 pins total for connection to carrier board

4. I/O DEFINITIONS

4.1 Location of Major Components

The figures below identify the major components and connectors found on the Open-Q 660 µSOM top and bottom sides.

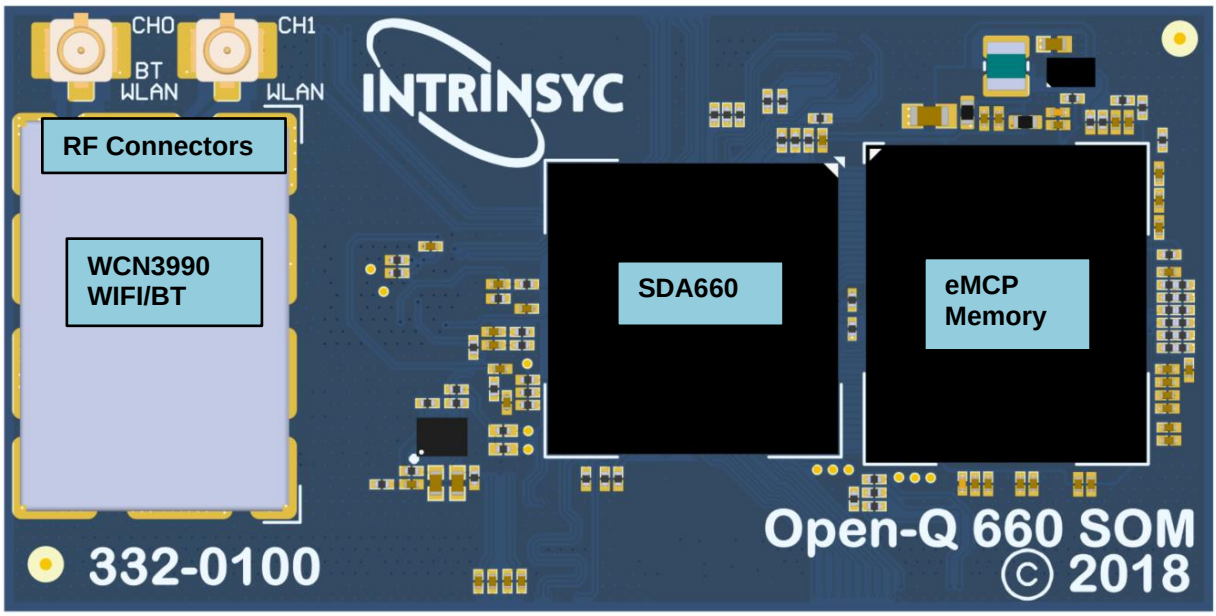

Figure 2 – Open-Q 660 µSOM Top View

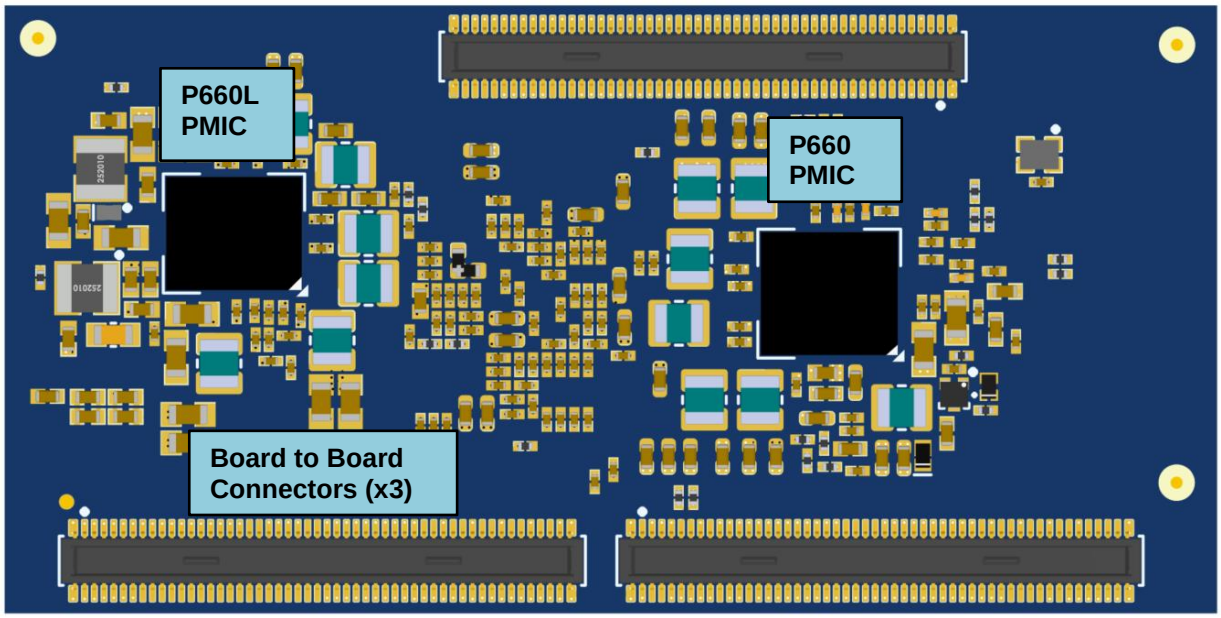

Figure 3 – Open-Q 660 µSOM Bottom View

The SOM mating connectors JT1, JT2, and JT3 are located on the bottom side of the SOM. The connector pin 1 locations are shown in the figure below (looking at bottom of SOM). Key dimensions are provided in later sections of this document.

The connectors are Hirose DF40C-100DP-0.4V(51). See section 6.3 for information on the available mating connectors.

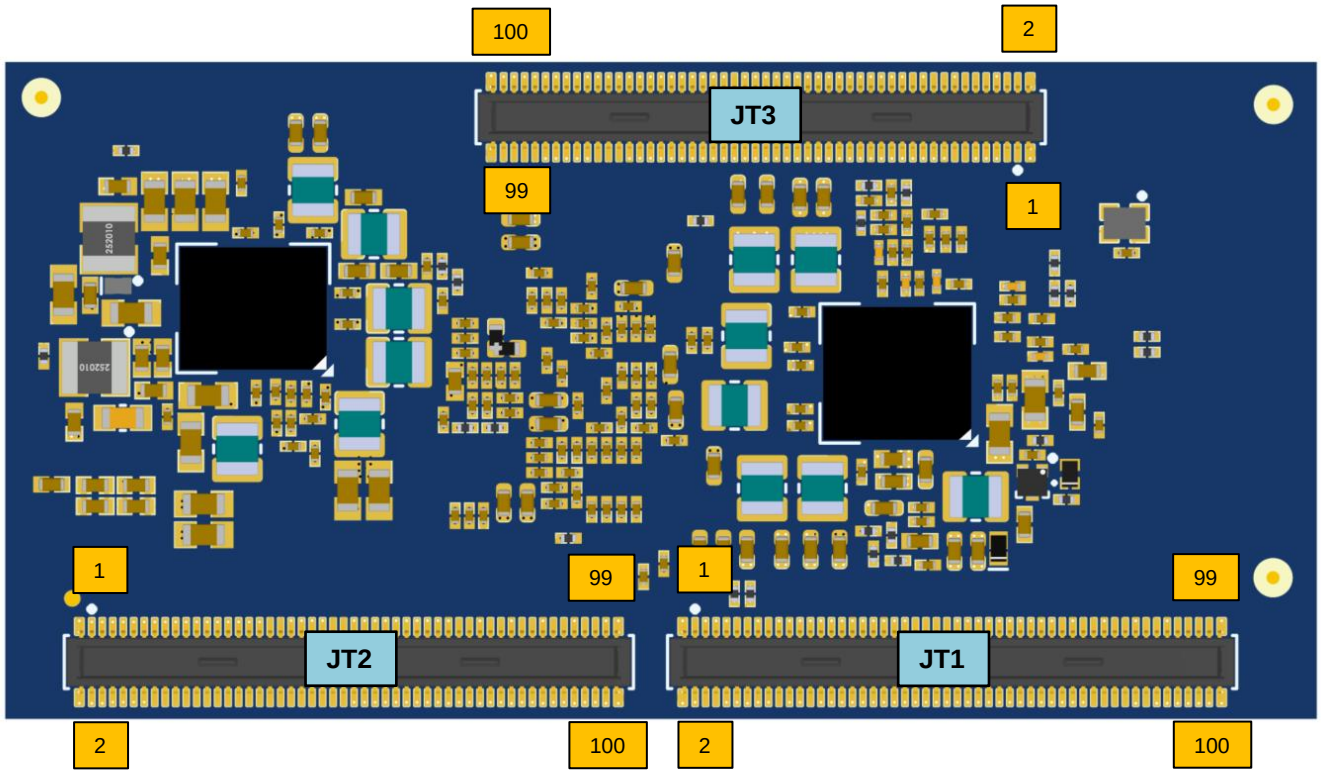

Figure 4 – Pin Locations of Board-to-Board Connectors

4.2 B2B Connector Signal Assignments

The following tables list the pin-outs of the three Open-Q 660 µSOM board to board connectors. A more detailed description of the signal group functions follows in the sections below. These descriptions provide the background information for customers developing a custom Carrier Board for the Open-Q 660 µSOM.

Note: the SOM schematic (document R-3) is the controlling document. In the event of pin-out difference(s) between this document and the SOM schematic, the SOM schematic shall take precedence.

Table 2 – B2B Connector JT1 Pin-outs

Pin #	Signal Name	Signal Name	Pin #
1	No Net	GPIO_113_DISP_ID	2
3	USB2_HS_D_P	No Net	4
5	USB2_HS_D_N	No Net	6
7	GND	USB1_SS_RX_N	8
9	USB1_HS_D_N	USB1_SS_RX_P	10
11	USB1_HS_D_P	GND	12
13	GND	USB1_SS_TX_N	14
15	No Net	USB1_SS_TX_P	16
17	PM660_GPIO_3_DIV_CLK_1	No Net	18
19	GND	USB0_SS_TX_N	20
21	GPIO_57_FORCED_USB_BOOT	USB0_SS_TX_P	22
23	GPIO_3_BLSP1_SPI_CLK	No Net	24
25	GPIO_1_BLSP1_SPI_MISO	GPIO_25_MI2S_2_WS	26
27	GPIO_2_BLSP1_SPI_CS_N	GPIO_24_MI2S_2_SCK	28
29	GPIO_0_BLSP1_SPI_MOSI	GPIO_63_LPG_WLED	30
31	GND	GPIO_68_ACCEL_INT	32
33	USB_SBU_N	GPIO_70_MAG_INT_N	34
35	USB_SBU_P	GPIO_77_SPKR_AMP_EN2	36
37	GND	GPIO_75_HALL_INT_N	38
39	USB0_SS_RX_N	GPIO_76_AUD_IO _GP3	40
41	USB0_SS_RX_P	GPIO_8_BLSP3_SPI_MOSI	42
43	HAP_OUT_N	GPIO_53_LCD_RESET_N	44
45	HAP_OUT_P	GPIO_67_TS_INT_N	46
47	No Net	GPIO_64_DISP_BL0_EN	48
49	CBL_PWR_N	GPIO_21_SNS_GP1	50
51	GPIO_51_CAM2_STANDBY_N	GPIO_4_BLSP2_UART_TX	52
53	GPIO_46_CAM0_RST_N	GPIO_5_BLSP2_UART_RX	54
55	GPIO_48_CAM2_RST_N	GPIO_97_BOOT_CONFIG1	56
57	GPIO_43_CAM_IRQ	GPIO_96_BOOT_CONFIG0	58
59	GPIO_52_PWR_SRC_DET	GPIO_98_BOOT_CONFIG2	60
61	GPIO_27_MI2S_2_D1	GPIO_92_CDC_RF_PA_ON	62
63	GPIO_26_MI2S_2_D0	GPIO_80_SPKR_AMP_EN1	64
65	RESOUT_N	GPIO_94_GRFC2_USER_BTN	66
67	GND	LPI_GPIO_7	68
69	PM660L_RGB_BLU	LPI_GPIO_6	70
71	PM660_KYPDPWR_N	GPIO_45_AUD_IO_EXP_1	72
73	GND	GPIO_42_MEMS_RESET_N	74
75	PM660_STAT_CHG	GPIO_50_CAM1_STANDBY_N	76
77	BATT_ID	No Net	78
79	GND	No Net	80
81	VBATT_SNS_N	No Net	82
83	VBATT_SNS_P	No Net	84
85	GND	PM660_RESIN_N	86
87	IBATT_SNS_P	QUIET_THERM	88
89	IBATT_SNS_N	GPIO_32_CAM_MCLK0	90
91	GND	GPIO_35_CAM_MCLK3	92
93	BATT_THERM	GPIO_34_CAM_MCLK2	94
95	VREG_L11A	GPIO_33_CAM_MCLK1	96
97	VREG_L14A	GPIO_31_AUD_IO_GP2	98
99	No Net	VREG_L2B	100

Table 3 – B2B Connector JT2 Pin-outs

Pin #	Signal Name	Signal Name	Pin #
1	SOM_SYS_PWR	GND	2
3	SOM_SYS_PWR	GND	4
5	SOM_SYS_PWR	SOM_SYS_PWR	6
7	SOM_SYS_PWR	SOM_SYS_PWR	8
9	SOM_SYS_PWR	SOM_SYS_PWR	10
11	SOM_SYS_PWR	SOM_SYS_PWR	12
13	SOM_SYS_PWR	PM660L_GP_4_CAM_REAR_ON	14
15	SOM_SYS_PWR	PM660L_GP_3_CAM_FRONT_ON	16
17	SOM_SYS_PWR	WLED_SINK3	18
19	SOM_SYS_PWR	WLED_SINK1	20
21	SOM_SYS_PWR	WLED_SINK2	22
23	SOM_SYS_PWR	VREG_WLED	24
25	USB_VBUS	CABC	26
27	USB_VBUS	PM660L_GP_5_USBA_VBUS_EN	28
29	USB_VBUS	VREG_L3B	30
31	USB_VBUS	VDISP_P_OUT	32
33	USB_VBUS	PM660L_KEY_VOL_UP_N	34
35	PM660L_RGB_RED	VDISP_M_OUT	36
37	PM660L_RGB_GREEN	SDC2_CLK	38
39	GPIO_54_SD_CARD_DET_N	SDC2_CMD	40
41	GPIO_73_HRM_INT	VREG_S5A	42
43	GPIO_74_CAP_INT_N	VREG_S5A	44
45	GPIO_61_MI2S_1_MCLK	VREG_S5A	46
47	FLASH_LED1	VREG_S5A	48
49	FLASH_LED2	GPIO_13_MI2S_1_WS	50
51	GPIO_20_AMP_PWR_EN	GPIO_12_MI2S_1_SCK	52
53	GPIO_9_BLSP3_SPI_MISO	GPIO_14_MI2S_1_D0	54
55	GPIO_10_BLSP3_SPI_CS_N	GPIO_15_MI2S_1_D1	56
57	GPIO_11_BLSP3_SPI_CLK_N	GPIO_69_GYRO_INT	58
59	GPIO_60_BOOT_CONFIG3	GPIO_71_ALSPG_INT_N	60
61	SDC2_DATA1	GPIO_72_FP_INT_N	62
63	SDC2_DATA0	GPIO_66_TS_RST_N	64
65	SDC2_DATA3	GPIO_59_MDP_VSYNC_P	66
67	SDC2_DATA2	GPIO_62_MI2S_2_MCLK	68
69	GND	GND	70
71	MIPI_DSI0_LANE3_P	MIPI_DSI1_LANE3_P	72
73	MIPI_DSI0_LANE3_N	MIPI_DSI1_LANE3_N	74
75	GND	GND	76
77	MIPI_DSI0_LANE2_P	MIPI_DSI1_LANE2_P	78
79	MIPI_DSI0_LANE2_N	MIPI_DSI1_LANE2_N	80
81	GND	GND	82
83	MIPI_DSI0_LANE1_P	MIPI_DSI1_LANE1_P	84
85	MIPI_DSI0_LANE1_N	MIPI_DSI1_LANE1_N	86
87	GND	GND	88
89	MIPI_DSI0_LANE0_P	MIPI_DSI1_LANE0_P	90
91	MIPI_DSI0_LANE0_N	MIPI_DSI1_LANE0_N	92
93	GND	GND	94
95	MIPI_DSI0_CLK_P	MIPI_DSI1_CLK_P	96
97	MIPI_DSI0_CLK_N	MIPI_DSI1_CLK_N	98
99	GND	GND	100

Table 4 – B2B Connector JT3 Pin-outs

Pin #	Signal Name	Signal Name	Pin #
1	USBC_CC1	VREG_L3B	2
3	USBC_CC2	VREG_L3B	4
5	GPIO_40_FLASH_FRONT_EN	VCOIN	6
7	GPIO_41_FL_STROBE_TRIG	GPIO_47_CAM1_RST_N	8
9	GPIO_49_AUD_IO_EXP_2	GPIO_37_CCI_SCL0	10
11	GPIO_22_BLSP6_I2C_SDA	GPIO_36_CCI_SDA0	12
13	GPIO_23_BLSP6_I2C_SCL	GND	14
15	GND	GPIO_44_CAM0_STANDBY_N	16
17	GPIO_29_AMP_RST_N	GPIO_30_AUD_IO_GP1	18
19	VREG_L5B	GND	20
21	VREG_L5B	GPIO_28_AMP_FAULT	22
23	VREG_L6B	GND	24
25	GPIO_38_CCI_SDA1	MIPI_CSI1_LANE3_P	26
27	GPIO_39_CCI_SCL1	MIPI_CSI1_LANE3_N	28
29	GND	GND	30
31	MIPI_CSI1_LANE0_P	MIPI_CSI1_LANE2_P	32
33	MIPI_CSI1_LANE0_N	MIPI_CSI1_LANE2_N	34
35	GND	VREG_L13A	36
37	MIPI_CSI1_CLK_N	MIPI_CSI1_LANE1_N	38
39	MIPI_CSI1_CLK_P	MIPI_CSI1_LANE1_P	40
41	GND	GND	42
43	MIPI_CSI2_CLK_P	MIPI_CSI0_CLK_P	44
45	MIPI_CSI2_CLK_N	MIPI_CSI0_CLK_N	46
47	GND	GND	48
49	MIPI_CSI2_LANE0_P	MIPI_CSI0_LANE0_P	50
51	MIPI_CSI2_LANE0_N	MIPI_CSI0_LANE0_N	52
53	GND	GND	54
55	MIPI_CSI2_LANE2_P	No Net	56
57	MIPI_CSI2_LANE2_N	GND	58
59	GND	MIPI_CSI0_LANE1_P	60
61	MIPI_CSI2_LANE3_P	MIPI_CSI0_LANE1_N	62
63	MIPI_CSI2_LANE3_N	GND	64
65	GND	MIPI_CSI0_LANE2_P	66
67	MIPI_CSI2_LANE1_P	MIPI_CSI0_LANE2_N	68
69	MIPI_CSI2_LANE1_N	GND	70
71	VREG_L13A	MIPI_CSI0_LANE3_P	72
73	VREG_L13A	MIPI_CSI0_LANE3_N	74
75	GND	GND	76
77	LPI_GPIO_21_AUD_SB_DATA1	LPI_GPIO_10_SPI_1_MOSI	78
79	LPI_GPIO_23_AUD_CDC_INT2	LPI_GPIO_11_SPI_1_MISO	80
81	LPI_GPIO_24_AUD_CDC_RSTN	LPI_GPIO_9_SPI_1_CLK	82
83	LPI_GPIO_17_MI2S_4_WS_CON	LPI_GPIO_3_I2C_3_SCL	84
85	LPI_GPIO_29_DMIC2_DATA	LPI_GPIO_2_I2C_3_SDA	86
87	LPI_GPIO_28_DMIC2_CLK	LPI_GPIO_15_UART_2_RX	88
89	LPI_GPIO_27_DMIC1_DATA	LPI_GPIO_14_UART_2_TX	90
91	LPI_GPIO_26_DMIC1_CLK	LPI_GPIO_1_PWR_EN	92
93	LPI_GPIO_22_AUD_CDC_INT1	LPI_GPIO_8_SPI_1_CS_N	94
95	LPI_GPIO_20_AUD_SB_DATA0	LPI_GPIO_0_SPI_1_CS1_N	96
97	LPI_GPIO_19_AUD_SB_CLK	LPI_GPIO_5	98
99	LPI_GPIO_18_WCD_SDM_MCLK	LPI_GPIO_4	100

4.3 Power Signals

See the table below for the power signal connections to the SOM.

NOTE: When the Pin # column shows '*', it indicates that there are multiple pins for that signal. See the B2B connector tables above for the full list of pin numbers.

Table 5 - Power Signal Connections

Connector	Pin #	Signal Name	Description
JT1, JT2, JT3	*	GND	Ground reference for the SOM
JT2	*	SOM_SYS_PWR	Main power source for SOM. Single cell Lithium battery connection or 3.8V DC power input.
JT2	*	USB_VBUS	USB VBUS connection. When used as power input, this is the charge power source for battery powered applications. For USB host mode applications, this is a power output.
JT3	6	VCOIN	Optional +3V rechargeable coin cell backup battery connection to SOM.
JT1	95	VREG_L11A	PM660 LDO11 +1.8V @ 150mA power output from SOM.
JT3	*	VREG_L13A	PM660 LDO13 +1.8V @ 600mA power output from SOM.
JT1	97	VREG_L14A	PM660 LDO14 +1.8V @ 150mA power output from SOM.
JT1	100	VREG_L2B	PM660L LDO2 +2.96V @ 50mA power output from SOM. Can be used for SD Card IO Voltage.
JT2,JT3	*	VREG_L3B	PM660L LDO3 +3.0V @ 600mA power output from SOM.
JT3	*	VREG_L5B	PM660L LDO5 +2.96V @ 600mA power output from SOM. Can be used for SD Card Supply Voltage.
JT1	23	VREG_L6B	PM660L LDO6 +3.3V @ 50mA power output from SOM.
JT2	*	VREG_S5A	PM660 Switcher 5 +1.35V @ 1200 mA power output from SOM.

4.4 Boot Control Signals

See the table below for the list of SOM boot / power on control signal connections.

Table 6 - SOM Control Signal Connections

Connector	Pin #	Signal Name	Description
JT1	65	RESOUT_N	APQ reset output used for indicating power on sequence.
JT1	49	CBL_PWR_N	Input for initiating auto power on sequence if desired.
JT1	21	GPIO_57_FORCED_USB_BOOT	APQ force USB boot input for factory programming during power on sequence / Configurable GPIO

JT1	58	GPIO_96_BOOT_CONFIG0	APQ watchdog disable input during power on sequence / Configurable GPIO
JT1	56	GPIO_97_BOOT_CONFIG1	APQ boot configuration input during power on sequence / Configurable GPIO
JT1	60	GPIO_98_BOOT_CONFIG2	APQ boot configuration input during power on sequence / Configurable GPIO
JT2	59	GPIO_60_BOOT_CONFIG3	APQ boot configuration input during power on sequence / Configurable GPIO
JT1	71	PM660_KYPDPWR_N	Power on button input for initiating power on sequence or reset.
JT1	86	PM660_RESIN_N	Volume down / reset button input.

4.5 Battery Related Signals

See the table below for the list of battery related control signal connections.

Table 7 - Battery Related Control Signal Connections

Connector	Pin #	Signal Name	Description
JT1	77	BATT_ID	Battery identification input.
JT1	93	BATT_THERM	Battery thermistor input.
JT1	89	IBATT_SNS_N	Battery current sense resistor input.
JT1	87	IBATT_SNS_P	Battery current sense resistor input.
JT1	75	PM660_STAT_CHG	Battery charge status / fault / interrupt output indicator.
JT1	81	VBATT_SNS_N	Battery voltage sense input.
JT1	83	VBATT_SNS_P	Battery voltage sense input.

4.6 GPIO Signals

See the table below for the list of GPIO signal connections.

Table 8 - GPIO Signal Connections

Connector	Pin #	Signal Name	Description
JT1	29	GPIO_0_BLSP1_SPI_MOSI	APQ Configurable GPIO / BLSP
JT1	25	GPIO_1_BLSP1_SPI_MISO	APQ Configurable GPIO / BLSP
JT1	27	GPIO_2_BLSP1_SPI_CS_N	APQ Configurable GPIO / BLSP
JT1	23	GPIO_3_BLSP1_SPI_CLK	APQ Configurable GPIO / BLSP
JT1	52	GPIO_4_BLSP2_UART_TX	APQ Configurable GPIO / BLSP
JT1	54	GPIO_5_BLSP2_UART_RX	APQ Configurable GPIO / BLSP
JT1	42	GPIO_8_BLSP3_SPI_MOSI	APQ Configurable GPIO / BLSP
JT2	53	GPIO_9_BLSP3_SPI_MISO	APQ Configurable GPIO / BLSP

JT2	55	GPIO_10_BLSP3_SPI_CS_N	APQ Configurable GPIO / BLSP
JT2	57	GPIO_11_BLSP3_SPI_CLK_N	APQ Configurable GPIO / BLSP
JT2	52	GPIO_12_MI2S_1_SCK	APQ Configurable GPIO / BLSP / MI2S
JT2	50	GPIO_13_MI2S_1_WS	APQ Configurable GPIO / BLSP / MI2S
JT2	54	GPIO_14_MI2S_1_D0	APQ Configurable GPIO / BLSP / MI2S
JT2	56	GPIO_15_MI2S_1_D1	APQ Configurable GPIO / BLSP / MI2S
JT2	51	GPIO_20_AMP_PWR_EN	APQ Configurable GPIO
JT1	50	GPIO_21_SNS_GP1	APQ Configurable GPIO
JT3	11	GPIO_22_BLSP6_I2C_SDA	APQ Configurable GPIO / BLSP
JT3	13	GPIO_23_BLSP6_I2C_SCL	APQ Configurable GPIO / BLSP
JT1	28	GPIO_24_MI2S_2_SCK	APQ Configurable GPIO / BLSP / MI2S
JT1	26	GPIO_25_MI2S_2_WS	APQ Configurable GPIO / BLSP / MI2S
JT1	63	GPIO_26_MI2S_2_D0	APQ Configurable GPIO / BLSP / MI2S
JT1	61	GPIO_27_MI2S_2_D1	APQ Configurable GPIO / BLSP / MI2S
JT3	22	GPIO_28_AMP_FAULT	APQ Configurable GPIO / BLSP
JT3	17	GPIO_29_AMP_RST_N	APQ Configurable GPIO / BLSP
JT3	18	GPIO_30_AUD_IO_GP1	APQ Configurable GPIO / BLSP
JT1	98	GPIO_31_AUD_IO_GP2	APQ Configurable GPIO / BLSP
JT1	90	GPIO_32_CAM_MCLK0	APQ Configurable GPIO
JT1	96	GPIO_33_CAM_MCLK1	APQ Configurable GPIO
JT1	94	GPIO_34_CAM_MCLK2	APQ Configurable GPIO
JT1	92	GPIO_35_CAM_MCLK3	APQ Configurable GPIO
JT3	12	GPIO_36_CCI_SDA0	APQ Configurable GPIO
JT3	10	GPIO_37_CCI_SCL0	APQ Configurable GPIO
JT3	25	GPIO_38_CCI_SDA1	APQ Configurable GPIO
JT3	27	GPIO_39_CCI_SCL1	APQ Configurable GPIO
JT3	5	GPIO_40_FLASH_FRONT_EN	APQ Configurable GPIO
JT3	7	GPIO_41_FL_STROBE_TRIG	APQ Configurable GPIO
JT1	74	GPIO_42_MEMS_RESET_N	APQ Configurable GPIO
JT1	57	GPIO_43_CAM_IRQ	APQ Configurable GPIO
JT3	16	GPIO_44_CAM0_STANDBY_N	APQ Configurable GPIO
JT1	72	GPIO_45_AUD_IO_EXP_1	APQ Configurable GPIO
JT1	53	GPIO_46_CAM0_RST_N	APQ Configurable GPIO
JT3	8	GPIO_47_CAM1_RST_N	APQ Configurable GPIO
JT1	55	GPIO_48_CAM2_RST_N	APQ Configurable GPIO
JT3	9	GPIO_49_AUD_IO_EXP_2	APQ Configurable GPIO / BLSP
JT1	76	GPIO_50_CAM1_STANDBY_N	APQ Configurable GPIO
JT1	51	GPIO_51_CAM2_STANDBY_N	APQ Configurable GPIO
JT1	59	GPIO_52_PWR_SRC_DET	APQ Configurable GPIO / BLSP
JT1	44	GPIO_53_LCD_RESET_N	APQ Configurable GPIO

JT2	39	GPIO_54_SD_CARD_DET_N	APQ Configurable GPIO / SD CARD DETECT
JT2	66	GPIO_59_MDP_VSYNC_P	APQ Configurable GPIO
JT2	45	GPIO_61_MI2S_1_MCLK	APQ Configurable GPIO / MI2S
JT2	68	GPIO_62_MI2S_2_MCLK	APQ Configurable GPIO / MI2S
JT1	30	GPIO_63_LPG_WLED	APQ Configurable GPIO
JT1	48	GPIO_64_DISP_BL0_EN	APQ Configurable GPIO
JT2	64	GPIO_66_TS_RST_N	APQ Configurable GPIO
JT1	46	GPIO_67_TS_INT_N	APQ Configurable GPIO
JT1	32	GPIO_68_ACCEL_INT	APQ Configurable GPIO
JT2	58	GPIO_69_GYRO_INT	APQ Configurable GPIO
JT1	34	GPIO_70_MAG_INT_N	APQ Configurable GPIO
JT2	60	GPIO_71_ALSPG_INT_N	APQ Configurable GPIO
JT2	62	GPIO_72_FP_INT_N	APQ Configurable GPIO
JT2	41	GPIO_73_HRM_INT	APQ Configurable GPIO
JT2	43	GPIO_74_CAP_INT_N	APQ Configurable GPIO
JT1	38	GPIO_75_HALL_INT_N	APQ Configurable GPIO
JT1	40	GPIO_76_AUD_IO _GP3	APQ Configurable GPIO
JT1	36	GPIO_77_SPKR_AMP_EN2	APQ Configurable GPIO
JT1	64	GPIO_80_SPKR_AMP_EN1	APQ Configurable GPIO
JT1	62	GPIO_92_CDC_RF_PA_ON	APQ Configurable GPIO
JT1	66	GPIO_94_GRFC2_USER_BTN	APQ Configurable GPIO
JT1	2	GPIO_113_DISP_ID	APQ Configurable GPIO
JT3	96	LPI_GPIO_0_SPI_1_CS1_N	APQ LPI Configurable GPIO
JT3	92	LPI_GPIO_1_PWR_EN	APQ LPI Configurable GPIO / Power Enable
JT3	86	LPI_GPIO_2_I2C_3_SDA	APQ LPI Configurable GPIO / I2C
JT3	84	LPI_GPIO_3_I2C_3_SCL	APQ LPI Configurable GPIO / I2C
JT3	100	LPI_GPIO_4	APQ LPI Configurable GPIO / BLSP
JT3	98	LPI_GPIO_5	APQ LPI Configurable GPIO / BLSP
JT1	70	LPI_GPIO_6	APQ LPI Configurable GPIO / BLSP
JT1	68	LPI_GPIO_7	APQ LPI Configurable GPIO / BLSP
JT3	94	LPI_GPIO_8_SPI_1_CS_N	APQ LPI Configurable GPIO / SPI
JT3	82	LPI_GPIO_9_SPI_1_CLK	APQ LPI Configurable GPIO / SPI
JT3	78	LPI_GPIO_10_SPI_1_MOSI	APQ LPI Configurable GPIO / SPI
JT3	80	LPI_GPIO_11_SPI_1_MISO	APQ LPI Configurable GPIO / SPI
JT3	90	LPI_GPIO_14_UART_2_TX	APQ LPI Configurable GPIO / UART
JT3	88	LPI_GPIO_15_UART_2_RX	APQ LPI Configurable GPIO / UART
JT3	83	LPI_GPIO_17_MI2S_4_WS_CON	APQ LPI Configurable GPIO / MI2S
JT3	99	LPI_GPIO_18_WCD_SDM_MCLK	APQ LPI Configurable GPIO / MI2S
JT3	97	LPI_GPIO_19_AUD_SB_CLK	APQ LPI Configurable GPIO / MI2S
JT3	95	LPI_GPIO_20_AUD_SB_DATA0	APQ LPI Configurable GPIO / MI2S

JT3	77	LPI_GPIO_21_AUD_SB_DATA1	APQ LPI Configurable GPIO / MI2S
JT3	93	LPI_GPIO_22_AUD_CDC_INT1	APQ LPI Configurable GPIO / MI2S
JT3	79	LPI_GPIO_23_AUD_CDC_INT2	APQ LPI Configurable GPIO / MI2S
JT3	81	LPI_GPIO_24_AUD_CDC_RSTN	APQ LPI Configurable GPIO
JT3	91	LPI_GPIO_26_DMIC1_CLK	APQ LPI Configurable GPIO / DMIC
JT3	89	LPI_GPIO_27_DMIC1_DATA	APQ LPI Configurable GPIO / DMIC
JT3	87	LPI_GPIO_28_DMIC2_CLK	APQ LPI Configurable GPIO / DMIC
JT3	85	LPI_GPIO_29_DMIC2_DATA	APQ LPI Configurable GPIO / DMIC
JT1	17	PM660_GPIO_3_DIV_CLK_1	PM660 Configurable GPIO / Clock output
JT2	16	PM660L_GP_3_CAM_FRONT_ON	PM660L Configurable GPIO
JT2	14	PM660L_GP_4_CAM_REAR_ON	PM660L Configurable GPIO
JT2	28	PM660L_GP_5_USBA_VBUS_EN	PM660L Configurable GPIO
JT2	34	PM660L_KEY_VOL_UP_N	Volume up button / PM660L Configurable GPIO_07

4.7 MIPI Signals

See the table below for the list of MIPI camera and display signals.

Table 9 - MIPI Serial Interface Signals

Connector	Pin #	Signal Name	Description
JT3	46	MIPI_CSI0_CLK_N	MIPI camera serial interface 0 clock
JT3	44	MIPI_CSI0_CLK_P	MIPI camera serial interface 0 clock
JT3	52	MIPI_CSI0_LANE0_N	MIPI camera serial interface 0 data lane 0
JT3	50	MIPI_CSI0_LANE0_P	MIPI camera serial interface 0 data lane 0
JT3	62	MIPI_CSI0_LANE1_N	MIPI camera serial interface 0 data lane 1
JT3	60	MIPI_CSI0_LANE1_P	MIPI camera serial interface 0 data lane 1
JT3	68	MIPI_CSI0_LANE2_N	MIPI camera serial interface 0 data lane 2
JT3	66	MIPI_CSI0_LANE2_P	MIPI camera serial interface 0 data lane 2
JT3	74	MIPI_CSI0_LANE3_N	MIPI camera serial interface 0 data lane 3
JT3	72	MIPI_CSI0_LANE3_P	MIPI camera serial interface 0 data lane 3
JT3	37	MIPI_CSI1_CLK_N	MIPI camera serial interface 1 clock
JT3	39	MIPI_CSI1_CLK_P	MIPI camera serial interface 1 clock
JT3	33	MIPI_CSI1_LANE0_N	MIPI camera serial interface 1 data lane 0
JT3	31	MIPI_CSI1_LANE0_P	MIPI camera serial interface 1 data lane 0
JT3	38	MIPI_CSI1_LANE1_N	MIPI camera serial interface 1 data lane 1
JT3	40	MIPI_CSI1_LANE1_P	MIPI camera serial interface 1 data lane 1
JT3	34	MIPI_CSI1_LANE2_N	MIPI camera serial interface 1 data lane 2
JT3	32	MIPI_CSI1_LANE2_P	MIPI camera serial interface 1 data lane 2
JT3	28	MIPI_CSI1_LANE3_N	MIPI camera serial interface 1 data lane 3
JT3	26	MIPI_CSI1_LANE3_P	MIPI camera serial interface 1 data lane 3

JT3	45	MIPI_CSI2_CLK_N	MIPI camera serial interface 2 clock
JT3	43	MIPI_CSI2_CLK_P	MIPI camera serial interface 2 clock
JT3	51	MIPI_CSI2_LANE0_N	MIPI camera serial interface 2 data lane 0
JT3	49	MIPI_CSI2_LANE0_P	MIPI camera serial interface 2 data lane 0
JT3	69	MIPI_CSI2_LANE1_N	MIPI camera serial interface 2 data lane 1
JT3	67	MIPI_CSI2_LANE1_P	MIPI camera serial interface 2 data lane 1
JT3	57	MIPI_CSI2_LANE2_N	MIPI camera serial interface 2 data lane 2
JT3	55	MIPI_CSI2_LANE2_P	MIPI camera serial interface 2 data lane 2
JT3	63	MIPI_CSI2_LANE3_N	MIPI camera serial interface 2 data lane 3
JT3	61	MIPI_CSI2_LANE3_P	MIPI camera serial interface 2 data lane 3
JT2	97	MIPI_DSI0_CLK_N	MIPI display serial interface 0 clock
JT2	95	MIPI_DSI0_CLK_P	MIPI display serial interface 0 clock
JT2	91	MIPI_DSI0_LANE0_N	MIPI display serial interface 0 data lane 0
JT2	89	MIPI_DSI0_LANE0_P	MIPI display serial interface 0 data lane 0
JT2	85	MIPI_DSI0_LANE1_N	MIPI display serial interface 0 data lane 1
JT2	83	MIPI_DSI0_LANE1_P	MIPI display serial interface 0 data lane 1
JT2	79	MIPI_DSI0_LANE2_N	MIPI display serial interface 0 data lane 2
JT2	77	MIPI_DSI0_LANE2_P	MIPI display serial interface 0 data lane 2
JT2	73	MIPI_DSI0_LANE3_N	MIPI display serial interface 0 data lane 3
JT2	71	MIPI_DSI0_LANE3_P	MIPI display serial interface 0 data lane 3
JT2	98	MIPI_DSI1_CLK_N	MIPI display serial interface 1 clock
JT2	96	MIPI_DSI1_CLK_P	MIPI display serial interface 1 clock
JT2	92	MIPI_DSI1_LANE0_N	MIPI display serial interface 1 data lane 0
JT2	90	MIPI_DSI1_LANE0_P	MIPI display serial interface 1 data lane 0
JT2	86	MIPI_DSI1_LANE1_N	MIPI display serial interface 1 data lane 1
JT2	84	MIPI_DSI1_LANE1_P	MIPI display serial interface 1 data lane 1
JT2	80	MIPI_DSI1_LANE2_N	MIPI display serial interface 1 data lane 2
JT2	78	MIPI_DSI1_LANE2_P	MIPI display serial interface 1 data lane 2
JT2	74	MIPI_DSI1_LANE3_N	MIPI display serial interface 1 data lane 3
JT2	72	MIPI_DSI1_LANE3_P	MIPI display serial interface 1 data lane 3

4.8 Interface Signals

See the table below for the list of signals for interfaces like USB and SDIO.

Table 10 - SDIO and USB Interface Signals

Connector	Pin #	Signal Name	Description
JT2	38	SDC2_CLK	Secure Digital IO clock
JT2	40	SDC2_CMD	Secure Digital IO command
JT2	63	SDC2_DATA0	Secure Digital IO data

JT2	61	SDC2_DATA1	Secure Digital IO data
JT2	67	SDC2_DATA2	Secure Digital IO data
JT2	65	SDC2_DATA3	Secure Digital IO data
JT1	33	USB_SBU_N	USB Sideband / DisplayPort
JT1	35	USB_SBU_P	USB Sideband / DisplayPort
JT1	39	USB0_SS_RX_N	USB SuperSpeed Receive Data (for Type C port)
JT1	41	USB0_SS_RX_P	USB SuperSpeed Receive Data (for Type C port)
JT1	20	USB0_SS_TX_N	USB SuperSpeed Transmit Data (for Type C port)
JT1	22	USB0_SS_TX_P	USB SuperSpeed Transmit Data (for Type C port)
JT1	9	USB1_HS_D_N	USB high speed data (for Type C port)
JT1	11	USB1_HS_D_P	USB high speed data (for Type C port)
JT1	8	USB1_SS_RX_N	USB SuperSpeed Receive Data (for Type C port)
JT1	10	USB1_SS_RX_P	USB SuperSpeed Receive Data (for Type C port)
JT1	14	USB1_SS_TX_N	USB SuperSpeed Transmit Data (for Type C port)
JT1	16	USB1_SS_TX_P	USB SuperSpeed Transmit Data (for Type C port)
JT1	5	USB2_HS_D_N	USB high speed data
JT1	3	USB2_HS_D_P	USB high speed data
JT3	1	USBC_CC1	OTG mode enable or CC1 pin for the USB Type-C connector
JT3	3	USBC_CC2	CC2 pin for the USB Type-C connector

4.9 Other Signals

The table below lists the remaining SOM signals.

Table 11 - Other Signals

Connector	Pin #	Signal Name	Description
JT2	26	CABC	Content adaptive backlight control input
JT2	47	FLASH_LED1	Flash LED Output 1 (300mA max)
JT2	49	FLASH_LED2	Flash LED Output 2 (300mA max)
JT1	43	HAP_OUT_N	Haptics H-bridge driver output
JT1	45	HAP_OUT_P	Haptics H-bridge driver output
JT1	69	PM660L_RGB_BLU	RGB LED Output: Blue Channel
JT2	37	PM660L_RGB_GREEN	RGB LED Output: Green Channel
JT2	35	PM660L_RGB_RED	RGB LED Output: Red Channel
JT1	88	QUIET_THERM	Temperature input to the analog MUX input, typically used for quiet thermistor readings
JT2	36	VDISP_M_OUT	Display Bias output
JT2	32	VDISP_P_OUT	Display Bias output
JT2	24	VREG_WLED	Backlight LED String Supply output
JT2	20	WLED_SINK1	Backlight LED String current sink 1

JT2	22	WLED_SINK2	Backlight LED String current sink 2
JT2	18	WLED_SINK3	Backlight LED String current sink 3

4.10 RF Antenna Connections

The Open-Q 660 µSOM provides WIFI and Bluetooth connectivity via the Qualcomm WCN3990 chipset. This provides 802.11 a/b/g/n/ac 2x2 MIMO, dual-band Wi-Fi, and Bluetooth 5.x. The 2x2 MIMO Wi-Fi requires two antennas for maximum throughput and operates at both 2.4GHz and 5GHz. Bluetooth uses only one of the antennas (CH0) and only operates at 2.4GHz. To support full performance of the Wi-Fi and Bluetooth, two dual-band antennas are required. If only Bluetooth is used, it can be supported with one single-band 2.4GHz antenna connected to the CH0 port.

The SOM uses two U.FL coaxial connectors (Hirose U.FL-R-SMT-1 (10)) for the antenna ports, as shown in the figure below.

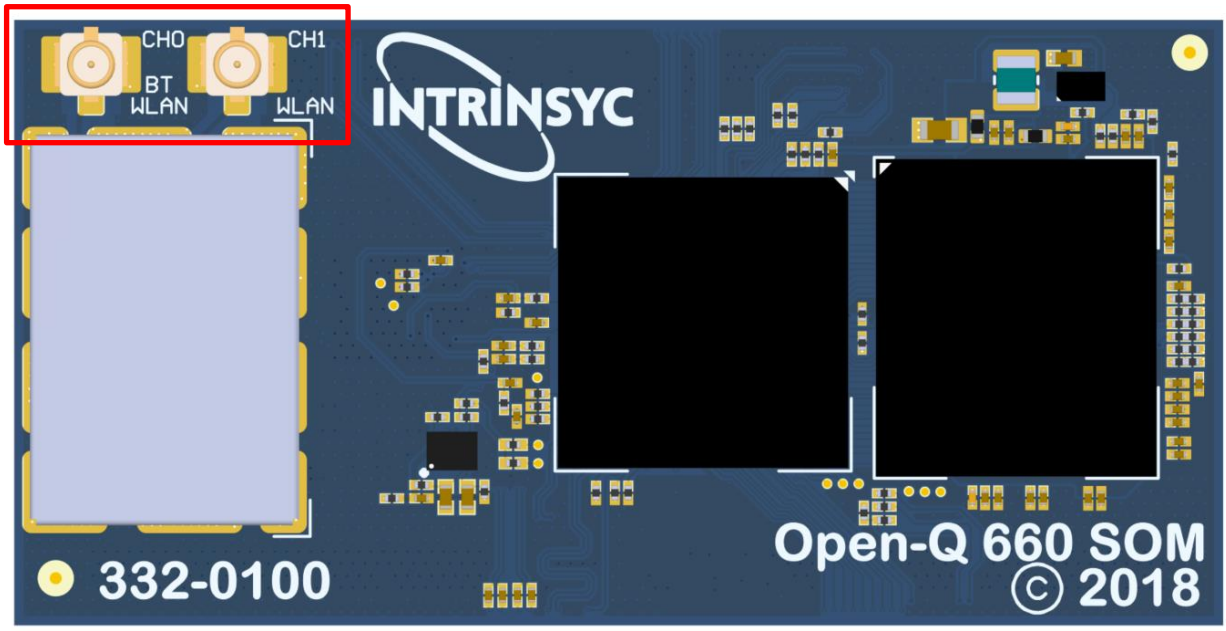

Figure 5 – Antenna Connection Locations on SOM

Table 12 – RF Signals via U.FL Coaxial Receptacles

Antenna	Description	Notes
Antenna CH0	RF chain 0 interface to Qualcomm WCN3990 chipset for Wi-Fi/BT	Antenna port for Wi-Fi and Bluetooth
Antenna CH1	RF chain 1 interface to Qualcomm WCN3990 chipset for Wi-Fi	Second antenna port for Wi-Fi 2x2 MIMO

5. ELECTRICAL SPECIFICATIONS

The input power to the SOM is provided by a power supply (battery or wall adapter) and also a USB source, for battery charging purposes. All input power sources enter the PM660 power management IC on the SOM, which then distributes power (along with the PM660L PMIC) to other circuits via LDO and switching power supply outputs.

5.1 Absolute Maximum Ratings

The table below shows the absolute maximum ratings in which the SOM input power sources can be exposed to without experiencing functional failure.

Table 13 – Absolute Maximum Input Power Ratings

Parameter	Min	Max	Units
Battery or DC power input (SOM_SYS_PWR)	-0.5	6	V
USB VBUS battery charger input voltage source (USB_VBUS)	-0.3	16	V

5.2 Operating Conditions

The table below shows the recommended operating conditions for the SOM to meet all performance specifications (provided the absolute maximum ratings have never been exceeded).

Table 14 – Operating Input Power Ratings

Parameter	Min	Typ	Max	Units
Battery or DC power input (SOM_SYS_PWR)	3.45[1]	3.8	4.75	V
USB VBUS battery charger input voltage source (USB_VBUS)	3.6	5	10	V
VCOIN Input	2.1	3.0	3.25	V

5.3 Operating Temperature

The SOM operating temperature ratings listed below are based only on the component case temperature ratings of individual components used on the SOM. Users should consider the specific environmental conditions in which the final product is used in.

Table 15 – Operating temperature range (Tc)

Parameter	Min	Typ	Max	Units
Overall SOM (case temperature)	-25	+25	+85	°C

[1] The SOM may be configured to operate at lower input voltage levels but changes to bootloader or proprietary code are needed and this will require support from Intrinsyc. Intrinsyc's solutions and software engineering services can provide advice and support for specialty low voltage requirements. Please contact Intrinsyc sales at: https://www.intrinsyc.com/sales-inquiry

5.4 Power Consumption

Power consumption tests have been done on the SOM under common operational modes. These results are outlined in the table below. All tests were executed at room temperature on the Open-Q 660 µSOM Development Kit running Android 9. The power consumption numbers listed in the table below reflect only what the SOM consumes during each operating mode.

Table 16 – Power Consumption Ratings

Operational Modes	Description	Average	Peak
Boot	Power consumption during boot process	N/A	5.4W
Suspend (Wi-Fi Off)	SOM placed in standby (Wi-Fi Off, Display Off)	13mW	N/A
Suspend (Wi-Fi On)	SOM placed in standby (Wi-Fi On, Display Off)	30mW	N/A
Idle (Display On)	SOM is idle (Wi-Fi Off, Display On)	0.32W	2.0W
Idle (Display Off)	SOM is idle (Wi-Fi Off, Display Off)	0.12W	1.6W
Video Record (1080P)	SOM recording 1080p video (Wi-Fi Off, Display On)	1.7W	3.6W
Video Record (4K UHD)	SOM recording 4K UHD video (Wi-Fi Off, Display On)	2.5W	4.1W
Video Playback (1080P)	SOM playing back 1080p video (Wi-Fi Off, Display On)	0.52W	2.4W
Video Playback (4K UHD)	SOM playing back 4K UHD video (Wi-Fi Off, Display On)	0.75W	2.6W
Audio Playback	SOM playing back MP3 audio file (Wi-Fi Off, Display Off)	0.14W	2.0W
Wi-Fi Download	SOM downloading data via Wi-Fi (Display Off)	1.8W	4.6W
Wi-Fi Upload	SOM uploading data via Wi-Fi (Display Off)	1.9W	3.3W
Full Load (All Cores)	SOM running all CPU cores (Wi-Fi Off, Display Off)	5.0W	6.0W
Single Core	SOM running single core (Wi-Fi Off, Display Off)	0.55W	1.4W
Bluetooth	SOM playing music over Bluetooth (Wi-Fi Off, Display Off)	0.18W	1.8W

5.5 ESD Ratings

The SOM is not designed with additional ESD protection other than what is included in the integrated circuits. It is recommended to take proper precautions in a static free environment when handling the SOM.

6. MECHANICAL SPECIFICATIONS

The sections below present some mechanical details of the Open-Q 660 µSOM. For access to the 3D design files, please see http://tech.intrinsyc.com/ (dev kit registration required).

6.1 SOM Mechanical Outline

The outer dimensions of the SOM are 50.0 x 25.0mm, as shown below.

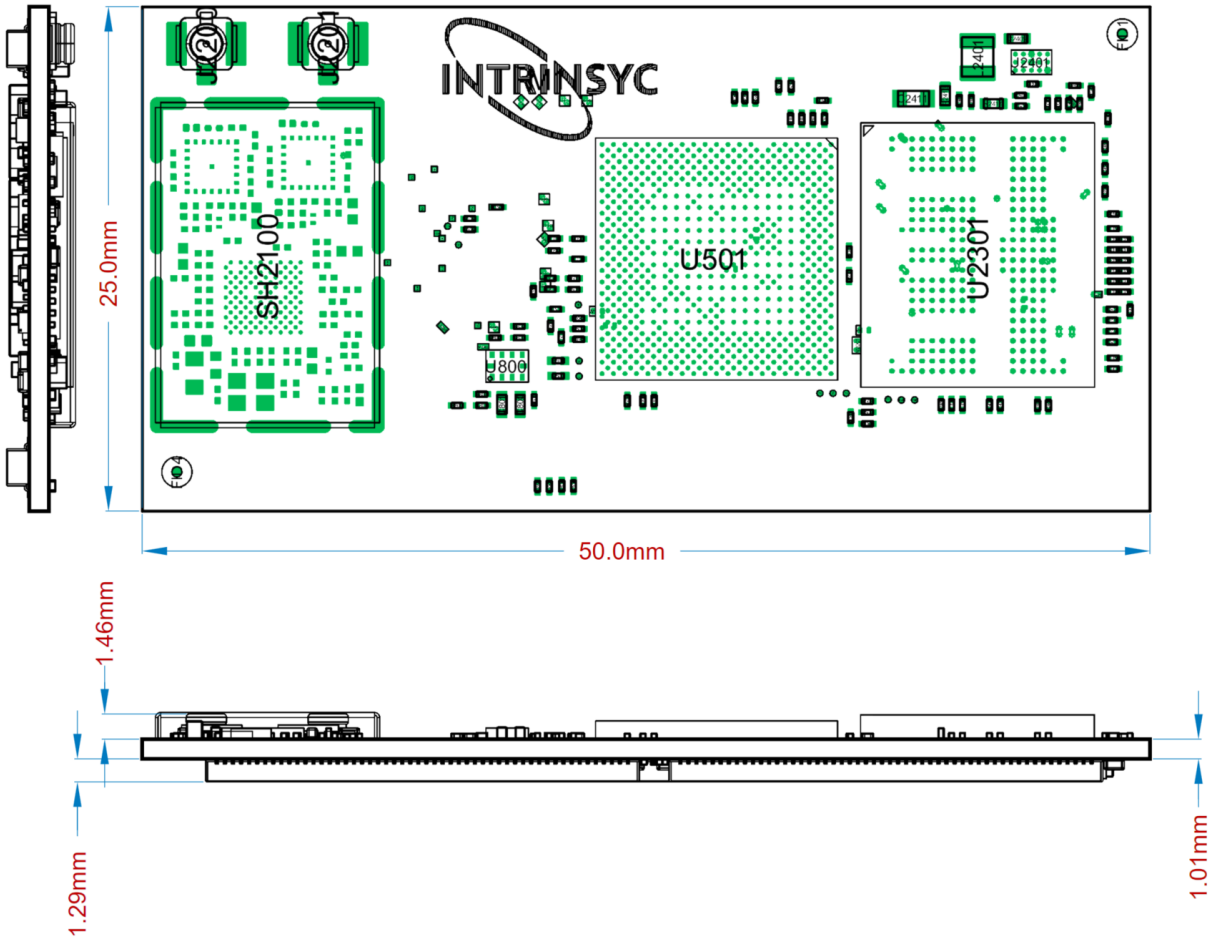

Figure 6 - SOM Mechanical Outline

6.2 Top and Bottom Height Restrictions

The tallest component on the top-side of the SOM is the WIFI shield at 1.46mm (see figure above). Please note that when the mating coax cables are connected, the top side height may be higher.

The tallest component on the bottom-side of the SOM are the board to board connectors at 1.29mm, otherwise the tallest components are 1mm tall.

6.3 Landing Pattern

Dimensions presented are in millimeters (mm). The footprint information in this section can be used as a guide when designing a landing area for the SOM.

Dimensions show the relative position of each connector on the SOM; referenced to the center of the connector body. NOTE: This information is given for reference. Please see SOM Carrier Board Design Guide for more detail (Reference document R-2).

*The perspective of this figure is looking through the top side of the SOM.

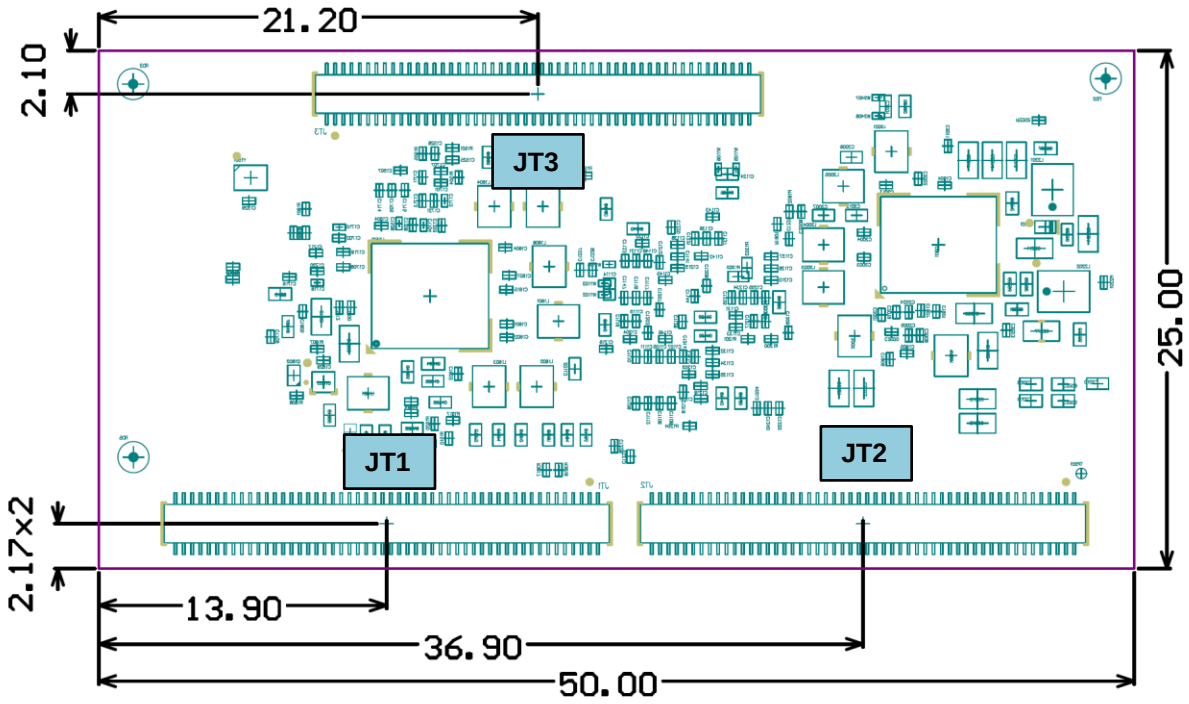

Figure 7 - SOM Land-Pattern Dimensions (mm)

The mating connector, Hirose DF40X-X-100DS-0.4V, is available in different heights, to achieve stack heights of 1.5mm or 3.0mm.

6.4 Thermal Characteristics

The SDA660 has built in thermal protections which will reduce processor frequency as the die temperature approaches set operating limits. These limits protect the APQ from damage that could be caused by elevated die temperature. Additional product-level thermal management will remove heat from the SOM and its components, allowing the APQ to run at higher frequencies for longer time periods before approaching the built in die temperature limits. This enables the average processor speed to remain higher through processor-intensive applications. Effectively removing heat from the 660 SOM is required to optimize system performance and efficiency and to ensure that the SDA660 can perform as desired.

For more information on thermal mitigation, see SOM Carrier Board Design Guide (Reference document R-2).

6.5 Weight

The SOM weighs approximately 6 grams.

6.6 B2B Connector Use Limit

The SOM board to board connectors JT1, JT2, and JT3 are designed to be removed and inserted for 30 cycles at most. It is recommended that users limit the number of times that a SOM is mated to a carrier board design.

7. PRODUCT MARKING, ORDERING, AND SHIPPING INFO

7.1 Product Marking

The SOM part number and product marking can be identified on the white label on the top of the module. The figure below shows an example of this label.

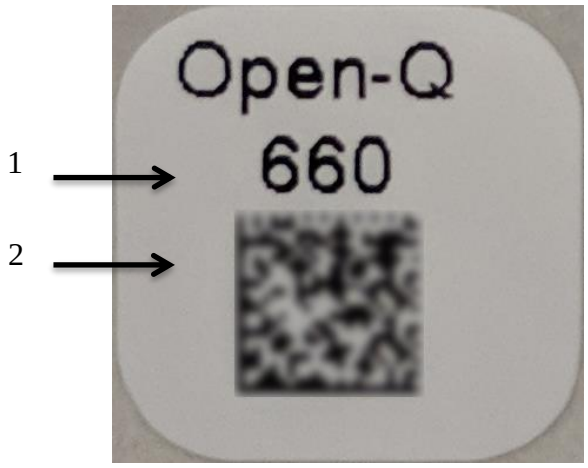

Figure 8 – Open-Q 660 µSOM Label (top of PCB)

Table 17 –Open-Q 660 µSOM Label Marking

Line	Marking	Description/ Notes
1	Open-Q 660	Intrinsyc Technologies product name
2	QR code *	Embeds serial number and Wi-Fi MAC address. The serial number format is VVV-WWXX-YYYYYY-ZZZZZ - VVV = Product number - WW = PCB revision number - XX = BOM revision number - YYYYYY = Date of manufacture (mm/dd/yy) - ZZZZZ = Unique serial number for PCB The MAC address format is 0123456789AB - 12 hexadecimal digit MAC address
* QR code reader mobile app (e.g. Neo Reader) can be used to read embedded serial number and the MAC address.		

7.2 Product Ordering Information

Orderable Part Numbers	
Open-Q 660 µSOM	QC-DB-N10004
Open-Q 660 µSOM Development Kit	QC-DB-N10003

The Open-Q 660 µSOM can be ordered for evaluation and prototype use from the Intrinsyc online store at http://shop.intrinsyc.com. For volume production orders or for custom requirements please contact Intrinsyc sales at https://www.intrinsyc.com/sales-inquiry.

7.3 Packaging and Shipping Information

The Open-Q 660 µSOM is packaged individually in small anti-static bags and bubble-wrap bags for protection during shipping. They are then put into different sized boxes depending upon the quantity of the order. Small quantities are shipped in standard courier boxes with bubble-wrap protection and large quantity orders are packaged in a carton with dividers. The figures below show examples of individual and large quantity SOM packaging.

Figure 9 - Individual SOM Packaging

Figure 10 - Packaging for Large Quantity Shipments

8. HANDLING PRECAUTIONS

8.1 ESD Precautions

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

The Open-Q 660 µSOM is designed as a component meant to be integrated into a final product and therefore has no additional ESD protection built-in. It should be handled only in a static-safe environment to prevent damage.

8.2 SOM – Carrier Board Mating Cautions

Caution must be taken when connecting or disconnecting the SOM to a carrier board to prevent damage. Ensure that the SOM is inserted and removed straight up and down to prevent any sideways force on the connectors which could damage them.

Also note that the DF40C-100DX board to board connectors are rated for a maximum of 30 mating / un-mating cycles. Therefore the number of insertions and removals must be limited to ensure reliability of the connectors.

8.3 Storage

The SOM must be stored in an antistatic bag.

9. CERTIFICATION

9.1 Radio Certification

The Intrinsyc Open-Q 660 µSOM is expected to be certified with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth. When certification is complete, the FCC and Industry Canada ID numbers will be listed here.

9.2 ROHS/REACH Compliance

The Intrinsyc Open-Q 660 µSOM is expected to comply with the ROHS/REACH standard. When compliance is complete, information on the ROHS/REACH certificate will be listed here.

10. COMPANY CONTACT

For more information, support or sales, please contact us.

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